

IN THE CLAIMS:

Claims 1 - 27 (**canceled**).

1 28. (**new**): A semiconductor memory cell including at least one transistor to
2 constitute the memory cell, the memory cell comprising:
3 a source region;
4 a drain region;
5 a body region disposed between and adjacent to the source region and the drain
6 region, wherein the body region is electrically floating; and
7 a gate disposed over the body region; and
8 wherein the memory cell includes:
9 a first data state representative of a first charge in the body region; and
10 a second data state representative of a second charge in the body region
11 wherein the second charge is substantially provided by removing charge from the
12 body region through the source region.

1 29. (**new**): The memory cell of claim 28 wherein the first charge is comprised of an
2 accumulation of majority carriers in the body region.

1 30. (**new**): The memory cell of claim 29 wherein the body region is comprised of a
2 P-type semiconductor material and the source and drain regions are comprised of an N-
3 type semiconductor material.

1 31. **(new)**: The memory cell of claim 29 wherein the majority carriers accumulate in
2 a portion of the body region that is adjacent to the source region.

1 32. **(new)**: The memory cell of claim 28 wherein positive voltages are applied to the
2 drain region and the gate to provide the second charge in the body region.

1 33. **(new)**: The memory cell of claim 28 wherein positive voltages are applied to the
2 drain region and the gate to remove at least the first charge from the body region.

1 34. **(new)**: The memory cell of claim 33 wherein, in response to positive voltages
2 being applied to the drain region and the gate, the memory cell includes a junction between
3 the body region and the source region, wherein the junction is forward biased.

1 35. **(new)**: The memory cell of claim 33 wherein, in response to the positive
2 voltages being applied to the drain region and the gate, the memory cell includes a forward
3 bias current between the body region and the source region.

1 36. **(new)**: The memory cell of claim 33 wherein the second charge is stored in the
2 body region in response to removing the positive voltages from the drain region and the
3 gate.

1 37. **(new)**: A semiconductor memory cell including at least one transistor to
2 constitute the memory cell, the memory cell comprising:

3 a source region having impurities to provide a first conductivity type;
4 a drain region having impurities to provide the first conductivity type,
5 a body region disposed between and adjacent to the source region and the drain
6 region wherein the body region is electrically floating and includes impurities to provide a
7 second conductivity type wherein the second conductivity type is different than the first
8 conductivity type;
9 a gate disposed over the body region,
10 wherein the memory cell includes:
11 a first data state representative of a first charge in the body region wherein
12 the first charge is substantially provided by impact ionization; and
13 a second data state representative of a second charge in the body region
14 wherein the second charge is substantially provided by removing charge from the
15 body region through the source region.

1 38. **(new)**: The memory cell of claim 37 wherein the first charge is comprised of
2 majority carriers and wherein the second conductivity type is a P-type.

1 39. **(new)**: The memory cell of claim 37 wherein, in response to a first positive
2 voltage applied to the drain region and a second positive voltage applied to the gate, at
3 least the first charge is removed from the body region through the source region.

1 40. **(new)**: The memory cell of claim 39 wherein the memory cell, in response to the
2 first and second positive voltages, includes a junction between the body region and the
3 source region which is forwarded biased.

1 41. **(new)**: The memory cell of claim 40 wherein the first conductivity type is an N-
2 type.

1 42. **(new)**: The memory cell of claim 41 wherein the second charge is stored in the
2 body region in response to removing the first positive voltage from the drain region before
3 removing the second positive voltage from the gate.

1 43. **(new)**: The memory cell of claim 41 wherein, in response to the first and second
2 positive voltages, the memory cell includes a forward bias current between the body region
3 and the source region.

1 44. **(new)**: The memory cell of claim 43 wherein the second charge is stored in the
2 body region in response to removing the first positive voltage from the drain region and the
3 second positive voltage from the gate.

1 45. **(new)**: The memory cell of claim 37 wherein the first charge is stored in the
2 body region in response to applying a first negative voltage to the drain region and a
3 second negative voltage to the gate.

1 46. **(new)**: The memory cell of claim 45 wherein the memory cell stores the first
2 charge in a portion of the body region that is adjacent to the source region.

1 47. **(new)**: A semiconductor memory cell including at least one transistor to
2 constitute the memory cell, the memory cell comprising:

3 a source region having impurities to provide a first conductivity type;
4 a drain region having impurities to provide the first conductivity type,
5 a body region disposed between and adjacent to the source region and the drain
6 region wherein the body region is electrically floating and includes impurities to provide a
7 second conductivity type wherein the second conductivity type is different than the first
8 conductivity type;

9 a gate spaced apart from, and capacitively coupled to, the body region,
10 wherein the memory cell includes:

11 a first data state representative of a first charge in the body region; and
12 a second data state representative of a second charge in the body region
13 wherein the second charge is substantially provided by removing charge from the
14 body region through the source region.

1 48. **(new)**: The memory cell of claim 47 wherein, in response to a first voltage
2 applied to the drain region and a second voltage applied to the gate, the first charge is
3 removed from the body region through the source region.

1 49. **(new)**: The memory cell of claim 48 wherein, in response to removing the first
2 voltage from the drain region before removing the second voltage from the gate, the
3 second charge is stored in the body region.

1 50. **(new)**: The memory cell of claim 48 wherein the second charge is stored in the
2 body region in response to applying ground to the drain region before removing the second
3 voltage from the gate.

1 51. **(new)**: The memory cell of claim 48 wherein the first voltage and the second
2 voltage are positive voltages which, during operation, are applied for a finite duration.

1 52. **(new)**: The memory cell of claim 48 wherein the memory cell, in response to the
2 first voltage and the second voltage, includes a junction between the body region and the
3 source region which is forward biased.

1 53. **(new)**: The memory cell of claim 52 wherein the first voltage and the second
2 voltage are positive voltages which are applied for a finite duration.

1 54. **(new)**: The memory cell of claim 53 wherein, in response to the positive
2 voltages being applied to the drain region and the gate, the memory cell includes a forward
3 bias current between the body region and the source region.

1 55. **(new)**: The memory cell of claim 54 wherein the memory cell stores the second
2 charge in the body region in response to a third voltage being applied to the drain region
3 before a fourth voltage is applied to the gate.

1 56. **(new)**: The memory cell of claim 55 wherein the third and fourth voltages are
2 ground.

1 57. **(new)**: The memory cell of claim 48 wherein the memory cell stores the first
2 charge in a portion of the body region that is adjacent to the source region.

1 58. **(new)**: The memory cell of claim 57 wherein the first charge is substantially
2 provided by impact ionization.

1 59. **(new)**: The memory cell of claim 48 wherein, in response to a first positive
2 voltage applied to the drain region and a second positive voltage applied to the gate, more
3 than the first charge is removed from the body region through the source region.

1 60. **(new)**: The memory cell of claim 59 wherein the first positive voltage is less
2 than the second positive voltage.